

CLAIMS

We claim:

- 1 1. A clock generator comprising:
 - 2 an input circuit adapted to selectively receive an input signal and modify a frequency of the input signal by a first programmable amount to generate a first input signal;
 - 5 a feedback loop circuit adapted to receive a feedback signal and modify a frequency of the feedback signal by a second programmable amount to generate a second input signal;
 - 8 a phase-locked loop core adapted to receive the first input signal and the second input signal and provide a first signal;
 - 10 a divider circuit adapted to receive the first signal and modify a frequency of the first signal to generate a plurality of second signals having programmable frequencies;
 - 13 an output circuit adapted to select from the plurality of second signals and provide at least one output signal; and
 - 15 a skew control circuit adapted to selectively apply skew to the output signal by a third programmable amount, wherein the first, second, and third programmable amounts and the programmable frequencies are determined by data selected from electrically erasable memory.

1 2. The clock generator of Claim 1, wherein the feedback
2 signal is selected from an internal feedback signal and an
3 external feedback signal, the skew control circuit further
4 adapted to selectively apply skew to the internal feedback
5 signal by a fourth programmable amount.

1 3. The clock generator of Claim 1, wherein the skew
2 control circuit may be selectively bypassed.

1 4. The clock generator of Claim 1, wherein the skew
2 comprises coarse adjustments or fine adjustments.

1 5. The clock generator of Claim 1, wherein the output
2 signal comprises two single-ended signals or a differential
3 signal, and the skew applied to each of the single-ended signals
4 by the skew control circuit may differ.

1 6. The clock generator of Claim 1, wherein a control
2 signal determines the data selected from the electrically
3 erasable memory.

1 7. The clock generator of Claim 1, further comprising
2 input/output boundary scan circuits adapted to provide JTAG test
3 support for the clock generator.

1 8. The clock generator of Claim 7, wherein the JTAG test
2 support provides IEEE 1149.1 compliance.

1 9. The clock generator of Claim 1, wherein the clock
2 generator is in-system programmable.

1 10. The clock generator of Claim 9, wherein the clock
2 generator is in-system programmable by supporting IEEE 1532
3 standards.

1 11. The clock generator of Claim 1, wherein the output
2 circuit is further adapted to provide the output signal over a
3 range of selectable voltage levels, signal types, and output
4 impedances, and the input circuit is further adapted to receive
5 the input signal having a possible range of voltage levels and
6 signal types.

1 12. An integrated circuit comprising:

2 means for selecting from a plurality of input signals and
3 generating a first input signal having a configurable frequency;

4 means for selecting from a plurality of feedback signals
5 and generating a second input signal having a configurable
6 frequency;

7 a phase-locked loop core adapted to receive the first input
8 signal and the second input signal and generate a first signal;

9 means for receiving the first signal and generating a
10 plurality of second signals having configurable frequencies;

11 means for selecting from the second signals and providing a
12 plurality of output signals; and

13 means for selectively skewing each of the output signals
14 and at least one of the feedback signals.

1 13. The integrated circuit of Claim 12, wherein the
2 skewing comprises coarse adjustments or fine adjustments.

1 14. The integrated circuit of Claim 12, further comprising
2 means for providing configurability and in-system
3 programmability.

1 15. The integrated circuit of Claim 12, further comprising
2 means for testing the integrated circuit to provide IEEE 1149.1
3 compliance.

1 16. The integrated circuit of Claim 12, further comprising
2 means for selecting the configurable frequency for the first
3 input signal and the second input signal and the configurable
4 frequencies for the second signals.

1 17. The integrated circuit of Claim 12, wherein the input
2 signals have a possible range of voltage levels and signal
3 types, and the output signals each have a programmable voltage
4 level and signal type.

1 18. The integrated circuit of Claim 17, wherein the signal
2 type comprises single-ended signals and differential signals.

1 19. A method of generating clock signals, the method
2 comprising:

3 receiving an input signal, wherein the input signal may be
4 a single-ended signal type or a differential signal type;

5 modifying a frequency of the input signal by an amount
6 determined from a first set of data selected from memory to
7 provide a first input signal;

8 receiving a feedback signal;

9 modifying a frequency of the feedback signal by an amount
10 determined from a second set of data selected from the memory to
11 provide a second input signal;

12 aligning a frequency and/or a phase of the first input
13 signal and the second input signal to provide a first signal;

14 modifying a frequency of the first signal to generate a
15 plurality of second signals having frequencies determined from a
16 third set of data selected from the memory;

17 selecting from the second signals a plurality of output
18 signals, which have programmable voltage levels and signal
19 types; and

20 applying skew to the output signals by an amount determined
21 from a fourth set of data selected from memory.

1 20. The method of Claim 19, wherein the amount of the skew
2 is based on coarse steps or fine steps.

1 21. The method of Claim 19, further comprising providing
2 in-system programmability to modify the first, second, third,
3 and fourth set of data stored in the memory.

1 22. The method of Claim 19, wherein a control signal
2 selects the first, second, third, and fourth set of data stored
3 in the memory.

1 23. The method of Claim 19, further comprising providing
2 JTAG compliant functional testing.

1 24. A clock generator comprising:

2 an input circuit adapted to receive an input signal and
3 provide the input signal to a phase-locked loop;

4 a phase-locked loop (PLL) adapted to receive the input
5 signal from the input circuit and to generate in response an
6 output signal;

7 an output circuit adapted to receive the output signal from
8 the PLL and provide the output signal as a clock signal;

9 a first skew control circuit coupled to the PLL and adapted
10 to generate a set of coarse skew adjustments and a set of fine
11 skew adjustments; and

12 a second skew control circuit programmable to select and
13 apply one of the skew adjustments to the output signal.

1 25. The clock generator of Claim 24, wherein the second
2 skew control circuit includes:

3 a plurality of registers programmable to store different
4 skew selection signals;

5 a first multiplexer coupled to the registers and adapted to
6 select one of the stored skew selection signals; and

7 a second multiplexer coupled to the first skew control
8 circuit and to the first multiplexer and adapted to select a
9 skew adjustment based on the skew selection signal selected by
10 the first multiplexer.

1 26. The clock generator of Claim 24, further comprising
2 input/output boundary scan circuits adapted to provide JTAG test
3 support.

1 27. The clock generator of Claim 24, wherein the clock
2 generator supports IEEE 1532 in-system programmable standards.

1 28. A method of generating clock signals, the method
2 comprising:

3 providing an input signal to a phase-locked loop (PLL);
4 generating with the phase-locked loop an output signal in
5 response to the input signal;
6 providing the output signal as a clock signal;
7 generating a set of coarse skew adjustments and a set of
8 fine skew adjustments; and
9 selecting and applying one of the skew adjustments to the
10 output signal.

1 29. The method of Claim 28, further comprising providing
2 JTAG compliant functional testing.

1 30. The method of Claim 28, further comprising providing
2 IEEE 1532 in-system programmability.